Remarks

Claims 1-13 are pending in this action and stand rejected. By this amendment claims 1, 8, 9, 10 and 12 have been amended and reconsideration of all pending claims is respectfully requested.

Claim Rejections - 35 U.S.C. § 102(e)

The Examiner rejected independent claims 1, 8, 9 and 10 under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 6,501,734 issued to Yu. The Examiner stated that Yu discloses a switching module, structure and system comprising various elements that correspond to the limitations recited in Applicants' independent claims herein. Applicants respectfully submit that Yu is directed to a structure and method to dynamically allocate bandwidth slots of an ***external*** memory between multiple data ports (Yu, Abstract; Col 4, lines 51-67; claims 1, 10 and 17) and not to a structure and system to route ATM based data packets to an ultimate destination node without modification of the packet header. (Applicants' Spec. Para. 0006, Abstract.) As such, Yu discloses a fundamentally different architecture then the present invention.

The Examiner stated, for example, that the Media Access Control (MAC) unit taught by Yu is equivalent to the first receiver of Applicants' invention, a limitation recited in each of Applicants' independent claims 1, 8, 9 and 10. (Final O.A. pp. 2-3) However, Applicants respectfully submit that the MAC unit of Yu implements a memory interface to support routing of data packets between Ethernet ports serving the workstation and the gigabit node. (Yu, Col. 4, lines 36-46) The MAC unit of Yu includes a memory interface unit that assigns low bandwidth ports to a fixed bandwidth slot of an **external** memory and dynamically allocates reserved bandwidth slots of the **external** memory to high bandwidth ports based on a memory allocation request. (Yu, Col. 2, lines 5-9, 15-18) Indeed, claims 1, 10 and 17 of Yu expressly recite an external memory interface to facilitate transfer of packet data between the switch and the external memory. The external memory of Yu is not integral to the ATM switch structure (Yu, Fig. 1, Col. 2, line 15-18, Col. 6,

lines 57-60) and therefore does not correspond to the limitation herein of a first or second memory integral to the first receiver, as currently amended. (Applicants' Spec. Para. 30 and Claims 1, 8, 9, and 10 ("... a first receiver which stores a first plurality of data packets in a first memory or a second memory ***integral to*** the first receiver ...").

More specifically, Applicants' receiver unit corresponds to the select data_in logical circuit 202. (Applicants' Spec. Par. 0022, Figs. 2 and 3) Each select data_in circuit contains eight identical "select data_in" logical blocks 203-1 to 203-8 (Applicants' Spec. Par. 0023, Fig. 2). The select data_in logical blocks include an internal memory 206 and an expansion memory 308. (Applicants' Spec. Par. 0030) The expansion memory of Applicants' first receiver (data_in select logic, 203-1) is used to store data packets with destination addresses outside the range of the primary switch module. (Applicants' Spec. Para. 30, Fig. 3) In this regard, Applicants assign a range of legal address values for each switching module and route received data packets, based on this assignment, to either the internal memory location or an expansion memory location – both residing ***within*** the data_in logical block (first receiver). Inasmuch as Applicants' recitation of a first receiver having a first memory and a second memory is not equivalent to the MAC unit of Yu, which is characterized by a memory interface that is coupled to an external memory, the Examiner's rejection is improper and should be withdrawn.

In addition, Yu teaches an internal rules checker (IRC) that outputs a forwarding descriptor to the switch subsystem for each frame to classify and communicate the priority of the data packet being processed. (Yu, Col. 5, lines 8-10 and 56-64.) The switching subsystem of Yu implements the frame forwarding decisions of the internal rules checker and requires a number of queues and dedicated cache and other hardware elements to perform the functions recited. (Yu, col. 5, lines 1-7 and 15-19) There being no counterpart for these elements in Applicants' invention, Yu does not anticipate the structure and system claimed herein to route ATM based data packets to an ultimate destination node without modification of the packet header.

In the Response to Arguments, the Examiner indicated the broadest reading of Applicants' independent claims 1, 8, 9 and 10 can be interpreted as "coupled to" since a memory "integral" to

the first or second receiver is not explicitly recited. Applicants have amended claims 1, 8-10 and 12 to recite a memory "integral to the first or second receiver." Claims 2-7 depend from claim 1 as amended. Claim 11 depends from claim 10 as amended. Therefore, Applicants respectfully submit that the Examiner's rejection of claims 1, 8-10 and 12 under 35 U.S.C. § 102(e) has been overcome.

Claim Rejections - 35 U.S.C. § 103(a), first paragraph

The Examiner rejected claims 2-7 and 11-13 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,501,734 to Yu in view of U.S. Pat. No. 5,689,500 to Chiussi. As noted above, Yu does not anticipate Applicants' invention because Yu expressly teaches and claims an external memory that services the ATM switch module while Applicants recite a memory integral to the first receiver. In addition, no motivation exists to combine Yu with Chiussi because Yu teaches a system for dynamically allocating bandwidth of an ATM switch based on priority (Yu, Col. 2, lines 5-9, 15-18) while Chiussi is directed to an ATM based switch architecture that handles multicast switching operations by **modifying** the ATM header. (Chiussi, Col. 4, lines 25-31 and 58-63) In this regard, Yu discloses a number of hardware elements to route ATM data that are obviated by Applicants' approach and Chiussi teaches a method that is inapposite to Applicants approach. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. (MPEP §2143.01) As such, a prima facie case of obviousness has not been established.

Applicants' claimed system and structure expressly avoids changing the packet address when it is necessary to change a switch module routing. (Applicants' Spec. Para. 0044) In other words, Applicants' invention routes the received data packets to their final destination ***without*** modifying the data packet header. (Applicants' Spec. Para. 0006, Abstract) Instead, Applicants assign a range of legal address values for each switch module and route received data packets, based on this assignment, to either the internal memory location or an expansion memory location of the data_in logical block. Accordingly, Chiussi, either alone or in combination with Yu, does

not suggest or motivate the data packet ranging and detection system disclosed by Applicants. Indeed, Chiussi teaches away from Applicants' approach because the invention herein requires no modification of the ATM cell header. Indeed, the multicast operation of Chiussi is implemented using an entirely different method from Applicants' invention. Accordingly, Applicants identify a second and independent grounds to patentably distinguish the prior art cited by the Examiner and respectfully traverse the rejection under 35 U.S.C. § 103(a).

The Examiner indicated that the broadest interpretation of independent claims 1, 8, 9, 10 and 12 can be interpreted as "coupled to" since "integrated" is not explicitly recited. Applicants have amended independent claims 1, 8, 9, 10 and 12 to recite a memory integral to the first or second receiver." Claims 2-7 depend from claim 1 as amended; claim 11 depends from claim 10 as amended; and Claim 13 depends from claim 12 as amended. Therefore, Applicants respectfully submit that the Examiner's rejection under 35 U.S.C. § 103(a) has been overcome.

Conclusion

Based on the foregoing, it is respectfully submitted that the pending claims in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

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